Acquisition Time Performance of a Novel Serial Search Acquisition Scheme for Chip-Asynchronous DS/SS Systems

RICHARD A. KORKOSZ
Electronic Systems Laboratory
GE Corporate Research & Development
Schenectady, New York 12301 USA

and

DILIP V. SARWATE
Coordinated Science Laboratory
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801 USA

ABSTRACT

We study the mean acquisition time performance of a novel serial search acquisition scheme for chip-asynchronous direct-sequence spread-spectrum systems. The sequences arising under the out-of-phase hypothesis are modeled as random sequences, and an appropriate likelihood ratio is computed in a sequential probability ratio test (SPRT) to test for the true phase of the received sequence. A different (and generally used) likelihood ratio is obtained for the SPRT if the out-of-phase sequences are modeled as zero sequences, and we use the performance under this model as a benchmark for comparison. An appropriate verification stage for the serial search scheme is designed based on fixed sample size (FSS) tests which employ the same likelihood ratio as used in the testing stage. A general expression for the mean acquisition time $E[T_{acq}]$ is derived, and the results indicate that the test statistic based on the random sequence model offers considerable savings in $E[T_{acq}]$ for moderate to large values of chip SNR.

1 Introduction

In a direct-sequence spread-spectrum (DS/SS) communication system, synchronization of the spreading code is usually achieved through two operations: acquisition and tracking [1, 2]. We only consider the acquisition process, in which the received code sequence and the locally generated replica of the code sequence are coarsely aligned within a fraction (usually one-half or less) of the chip duration. The acquisition problem has been studied extensively in the literature, and several different acquisition schemes have been proposed [1, 2]. We only consider the class of serial search schemes in which employ a single correlator is used to test one phase at a time.

Most traditional serial acquisition schemes are designed based on the assumption that no signal is present under the out-of-phase hypothesis, i.e., the sequences appearing under this hypothesis are modeled as zero sequences. However, it was recently shown that better performance can be obtained if the out-of-phase signal component is modeled via a random sequence model rather than ignored [3]-[7]. In particular, the results in [3, 4] were obtained for chip-synchronous systems in which the location of the chip boundaries of the received code waveform are known to the receiver. Since such an assumption may not always be very realistic, we consider the more general chip-asynchronous model in which the chip boundaries of the received code waveform are not known to the receiver. A novel serial search acquisition scheme for chip-asynchronous systems was introduced in [5, 6], and it was shown that improved performance at the testing stage can be obtained if a sequential probability ratio test (SPRT) based on the random sequence model (rather than the zero sequence model) is employed. The goal of the present paper is to determine the extent to which these different approaches affect the mean acquisition time.

The remainder of this paper is organized as follows. In Section 2 we describe the coherent chip-asynchronous system model introduced in [5]-[7], and also briefly summarize the serial acquisition schemes and observation models considered. The serial search scheme employs both a testing stage and a verification stage, and each is described in further detail in Section 3 and 4, respectively. In particular, we design the testing and verification stages for both the random sequence and zero sequence models. Based on the performance parameters of the testing and verification stages, an expression for the mean acquisition time is derived in Section 5, where some numerical results are also provided. Finally, conclusions are discussed in Section 6.

2 System Model

Let the code sequence $\{c^{(0)}\} = \{\ldots, c^{(0)}(0), c^{(0)}(1), c^{(0)}(2), \ldots\}$ be a pseudonoise (PN) sequence (that is, a maximal-length shift register sequence) with period $L$ and elements $c^{(0)}(j) \in \{-1, 1\}$, and let $c(t) = \sum_{j=-\infty}^{\infty} c^{(0)}(j) \Pi_{T_c}(t - jT_c)$ denote the corresponding pulse train, where $\Pi_{T_c}(\cdot)$ is the rectangular pulse function of duration $T_c$ centered at $T_c/2$. The $k^{th}$ phase of $\{c^{(0)}\}$ is its $k^{th}$ left shift $\{c^{(k)}\}$, where $c^{(k)}(i) = c^{(0)}(i + k), i = \ldots, -2, -1, 0, 1, 2, \ldots$. We assume that the receiver is perfectly synchronized to the received RF carrier both in frequency and in phase, and that no data modulation is present in the received signal during the acquisition process. Thus, without loss of generality, we consider the baseband model

$$r(t) = \sqrt{V} c(t + \delta T_c) + n(t)$$

(1)

for the received signal, where $V$ denotes the received signal power, $\delta T_c$ is the unknown time shift, and $n(t)$ is additive white Gaussian noise with two-sided power spectral density $N_0/2$. Since $c(t)$ is periodic with period $LT_c$, there is no loss of generality in assuming that $\delta \in [0, L)$. Let $\delta = k + \epsilon$, where $k = \lfloor \delta \rfloor$ and $0 \leq \epsilon < 1$. Then (1) can be written as

$$r(t) = \sqrt{V} \sum_{l=-\infty}^{\infty} c^{(k)}(l) \Pi_{T_c}(t - lT_c + \epsilon T_c) + n(t),$$

(2)

where $k \in \{0, 1, \ldots, L - 1\}$ is the unknown phase of the received signature sequence and $\epsilon \in [0, 1)$ is the unknown fractional chip offset. The model in (2) is called the coherent chip-asynchronous model.

Now, the acquisition problem is that of aligning the local code waveform with the received code waveform to within some prescribed accuracy of $\pm \zeta$ chips, where the value of $\zeta$ depends on the pull-in range of the code tracking loop (we assume that...
\( \zeta \leq \frac{1}{2} \). Equivalently, the goal of acquisition is to obtain an estimate \( \delta \in [0, L) \) of the unknown time offset \( \delta \) such that \( \min \{ (\delta - \delta), L - | \delta - \delta | \} \leq \zeta \). Our approach for estimating \( \delta = k + \xi \) is to obtain separate estimates \( \hat{k} \) and \( \hat{\xi} \) of \( k \) and \( \xi \), respectively, where \( \hat{k} \in \{0, 1, \ldots, L - 1\} \) and \( \hat{\xi} \in [0, 1) \) [5]-[7]. Then the estimate \( \hat{\delta} \) is given by \( \hat{\delta} = \hat{k} + \hat{\xi} \). In the present paper we consider only estimation of \( \delta \) via serial search, while the estimation of \( \xi \) is considered elsewhere [8, 7].

Often the receiver may know ahead of time that only \( L' \) possible phases may be received, where \( L' < L \). Thus, without loss of generality we may write the set of possible received phases as \( \{0, 1, \ldots, L' - 1\} \). This set of phases is called the uncertainty region, and the search scheme need only search over phases in the uncertainty region. We assume that each possible phase in the uncertainty region has a priori probability \( 1/L' \).

Since the priors are equal, the order in which the serial search scheme tests the \( L' \) possible phases is irrelevant to the acquisition time performance. Thus, we assume without loss of generality that the phases are tested in increasing order as follows. First, the receiver generates the local code waveform \( c(t) \) and compares \( c(t) \) with the received signal \( r(t) = \sqrt{V} c(t + kT_c + \xi T_c) + n(t) \) for several chip times in order to decide whether \( k = 0 \). If the receiver decides that \( k \neq 0 \), it generates \( c(t + T_c) \) and compares it with \( r(t) \) in order to decide whether \( k = 1 \), and so on, ... until for some \( i \), the receiver decides that \( k = i \). The receiver hopes that (with high probability) this decision is correct and the phase of the sequence has been acquired. The design of an effective testing stage is described in further detail in Section 3.

Most of the comparisons of \( c(t + iT_c) \) with \( r(t) \) result in the decision that \( k \neq i \). Since a large number of incorrect cells must typically be searched before the correct cell is reached, it is important to decide on such rejections quickly, that is, after comparing the signals over relatively few chip intervals. On the other hand, the short observation intervals can result in unreliable decisions. In particular, this testing stage may accept the current phase \( i \) even though \( k \neq i \). Because of this problem, a verification stage is employed in which the decision to accept the current phase is tested over a relatively long time interval of (fixed) length \( T_{ver} \). Since \( T_{ver} \) is finite, the verification stage is not error-free. However, \( T_{ver} \) may be chosen large enough so that the verification stage has negligibly small error probability. The design of an adequate verification stage is described in further detail in Section 4. The serial acquisition model described above is illustrated by the state diagram in Figure 1.

Suppose that the receiver wishes to test whether \( k \), the unknown incoming phase, is the same as \( i \), the phase of the locally generated sequence. As in [5]-[7], the received signal \( r(t) \) is correlated with the locally generated code signal \( c(t + iT_c) \) over successive chip intervals \( jT_c, (j + 1)T_c \). Suitably normalized, the \( j \)th observation is

\[
Z(j) = p (1 - e^{-j}) + c^{(j)}(j + 1) + W(j),
\]

where \( p = \sqrt{2} T_c / N_a \) is a measure of the chip signal-to-noise ratio, and \( \{ W(j) \} \) is a sequence of independent and identically distributed (i.i.d.) standard (that is, zero-mean, unit variance) Gaussian random variables. As described in [5]-[7], we only consider the observations \( \{ Z(j) : j \in S_i \} \) to decide between the two hypotheses

\[
\begin{align*}
H_0 & : k = i \quad \text{(in-phase hypothesis)} \\
H_1 & : k \neq i \quad \text{(out-of-phase hypothesis)},
\end{align*}
\]

where \( S_i = \{ j \geq 0 : \epsilon^{(j)}(j) = \epsilon^{(j)}(j + 1) \} \). This is motivated by the fact that the observations \( \{ Z(j) : j \in S_i \} \) do not depend on \( \epsilon \) under the in-phase hypothesis. The remaining observations depend on \( \epsilon \) and may be used to estimate \( \epsilon \) simultaneously with the operation of the serial search scheme [6, 7]. It is shown in [5, 7] that (3) can be written as

\[
Z(j) = \begin{cases} 
p + W(j) & \text{if } k = i \\
(1 - e^{(j)}) + c^{(j+1)}(j + 1) + W(j) & \text{if } k = i - 1 \\
(1 - e^{(j)}) + c^{(j+1)}(j + 1) + W(j) & \text{otherwise}
\end{cases}
\]

for \( j \in S_i \), where \( l \) is different from both \( k \) and \( i \) and \( l' \) is different from both \( k \) and \( i - 1 \). Due to the complicated form of the observations under the out-of-phase hypothesis, simpler models were considered for testing \( H_1 \) versus \( H_0 \), namely the random sequence model and the zero sequence model [5, 7].

The random sequence model is based on modeling the PN sequences appearing under the out-of-phase hypothesis as random Bernoulli sequences. With this model, the observations \( \{ Z(j) : j \in S_i \} \) can be modeled as

\[
Z(j) = \begin{cases} 
p + W(j) & \text{if } k = i, \text{i.e. if } H_1^{(1)} \text{ is true} \\
X(j) + W(j) & \text{if } k \neq i, \text{i.e. if } H_0^{(1)} \text{ is true}
\end{cases}
\]

where \( X(j) \) takes on the four values \( \pm 1 \) and \( \pm (1 - 2\epsilon) \) with equal probability independently of the noise sequence \( \{ W \} \) [5, 7]. The notation \( H_1^{(1)} \) in (3) is used to indicate hypothesis \( H_1 \) under the random sequence model.

Similarly, the zero sequence model is based on modeling the PN sequences appearing under the out-of-phase hypothesis as zero sequences. In this case, the observations \( \{ Z(j) : j \in S_i \} \) are modeled as

\[
Z(j) = \begin{cases} 
p + W(j) & \text{if } k = i, \text{i.e. if } H_1^{(2)} \text{ is true} \\
W(j) & \text{if } k \neq i, \text{i.e. if } H_0^{(2)} \text{ is true}
\end{cases}
\]

where \( H_1^{(2)} \) indicates hypothesis \( H_1 \) under the zero sequence model.

The design and performance of testing stages based on the models in (4) and (5) are considered in Section 3. Similarly, in Section 4 we consider the design and performance of verification stages based on the random sequence and zero sequence models. In Section 5 we derive the mean acquisition time \( E[T_{acq}] \) for the proposed serial search schemes and compare some numerical results.

3 Testing Stage Design

The purpose of the testing stage is to decide between the hypotheses \( H_0 (k \neq i) \) and \( H_1 (k = i) \). In general, since we wish to acquire the incoming phase rapidly, we would like to decide between the two hypotheses as quickly as possible, subject to specified error probabilities. Thus, sequential probability ratio tests (SPRT's) are considered for use in the testing stage. In particular, we consider the two cases where the SPRT is based on the random sequence and zero sequence models in (4) and (5). These tests were studied in [5, 7], and are briefly summarized in the following.

As in [5], we use the superscripts (1) and (2) to denote the test parameters based on the random sequence model (resp., zero sequence model). For a fixed local phase \( i \), we denote the observations fed to the SPRT, \( \{ Z(j) : j \in S_i \} \), as \( \{ U(m) : m = 0, 1, \ldots \} \).
Then, the SPRTs \( \Psi^{(\ell)}(A^{(\ell)}, B^{(\ell)}) \) \( \ell = 1, 2 \) may be described as follows:

Sample \( (U(0), U(1), \ldots) \) sequentially until the random time \( N^{(\ell)} \) given by

\[
N^{(\ell)} = \inf \left\{ n \geq 1 : \left[ \prod_{m=0}^{n-1} A^{(\ell)}(U(m)) \right] \not\in (A^{(\ell)}, B^{(\ell)}) \right\},
\]

where

\[
A^{(\ell)}(z) = \frac{4\phi(z - p)}{\phi(z - p) + \phi(z + p) + p^{-1}[\Phi(z + p) - \Phi(z - p)]}
\]

is the likelihood ratio derived (as explained in [5, 7]) under the random sequence model in (5),

\[
A^{(\ell)}(z) = \exp(\rho z - p^2/2).
\]

The performance of the tests \( \Psi^{(1)} \) and \( \Psi^{(2)} \) was evaluated in [5, 7] for the case where the observations are distributed according to the random sequence model in (5), and also for the case where the observations are distributed according to actual PN sequences as in (4). The numerical results were conditioned on various fixed values of the unknown fractional offset \( \epsilon \). In all of these cases it was proven that the stopping variable \( N^{(\ell)} \) is exponentially bounded for \( \ell = 1, 2 \), any \( \epsilon \in [0, 1] \), and any \( p > 0 \) [7]. In particular, all moments of \( N^{(\ell)} \) are finite, and \( P[N^{(\ell)} < \infty] = 1 \) for \( \ell = 1, 2 \) so that both tests terminate with probability one.

The performance of the tests \( \Psi^{(1)} \) and \( \Psi^{(2)} \) under the hypotheses in (5) for fixed \( p \) and \( \epsilon \) is denoted as follows. We write \( \alpha^{(\ell)} = P[\Psi^{(\ell)}(A^{(\ell)}, B^{(\ell)}) \text{ chooses } H_1^{(1)} | H_0^{(1)} \text{ is true}] \) and \( \beta^{(\ell)} = P[\Psi^{(\ell)}(A^{(\ell)}, B^{(\ell)}) \text{ chooses } H_0^{(2)} | H_1^{(2)} \text{ is true}] \), respectively, to denote the probabilities of false alarm and missed detection for the test \( \Psi^{(\ell)}(A^{(\ell)}, B^{(\ell)}) \) \( \ell = 1, 2 \). The corresponding average sample numbers (ASN) of the tests are denoted \( E^{(1)}[N^{(\ell)}] = E[N^{(\ell)} | H_0^{(1)}] \) and \( E^{(2)}[N^{(\ell)}] = E[N^{(\ell)} | H_1^{(2)}] \). These quantities may be computed once the thresholds \( A^{(\ell)}, B^{(\ell)} \) and the parameters \( p \) and \( \epsilon \) are specified. It was shown in [5, 7] that \( \alpha^{(2)} \) is usually significantly larger than \( \alpha^{(1)} \), while the other three performance parameters are similar for the two tests. Moreover, it was observed that the performance degradation in the false alarm error probability is an increasing function of the chip SNR. Thus, it is useful to study how this degradation affects the mean acquisition time, and this is done in Section 5.

4 Verification Stage Design

The purpose of the verification stage is to check the decision made at the testing stage whenever the in-phase hypothesis is declared. Ideally, we would like the verification process to be error free, but this is not possible in a practical system. Thus, as in [4, 7, 8], we assume that an error probability specification \( \text{Pe}_{\text{err}} \) is given and design the testing stage so that the error probabilities do not exceed this specified value. We only consider fixed sample size (FSS) tests for the testing stage which compare the log-likelihood ratio of the observations to a threshold. Since our purpose is to compare the mean acquisition time for serial search schemes based on the random sequence and zero sequence models, it is appropriate that the verification stage in each case employs the same likelihood ratio as used in the testing stage. Thus, if the testing stage uses the likelihood ratio \( \Lambda^{(\ell)}(\cdot) \) in (8) or (9), the corresponding FSS test in the verification stage is

Choose \( H_1^{(2)} \) if \( \sum_{m=n}^{m+n} \log \Lambda^{(\ell)}(U(m)) > 0 \) and \( H_0^{(2)} \) otherwise.

Here we assume that the observations \( \{U(m) : m = 0, 1, \ldots \} = \{Z(j) : j \in S_i \} \) are distributed according to the random sequence model as in (5), and choose the integers \( T^{(\ell)}_\text{err} \) \( \ell = 1, 2 \) so that the error probability under each hypothesis is smaller than the given specification \( \text{Pe}_{\text{err}} \).

In general we would like to choose \( T^{(\ell)}_\text{err} \) as small as possible such that the given error probability specification is satisfied. This can be done by using a Chernoff bounding approach as in [4, 8], except now the problem is complicated by the fact that the distribution of the observations under \( H_0^{(2)} \) in (5) depends on \( \epsilon \), which is unknown. Moreover, neither of the likelihood ratios used in the FSS test is matched to the distribution of the observations. Nevertheless, consider the case where the verification stage is given by (10) with \( \ell = 1 \), so the test based on the random sequence model with likelihood ratio \( \Lambda^{(1)}(\cdot) \) in (8) is used. It can be shown [7] via a Chernoff bound and some additional analysis that for any fixed \( \epsilon \in [0, 1] \), both of the verification error probabilities are bounded from above by the quantity

\[
\left( \min_{\epsilon \in [0, 1]} \int_{-\infty}^{\infty} [\Lambda^{(1)}(y)]^{4} \left[ \phi(y - p) + \phi(y + p) + 2\phi(y) \right] dy \right)^{\tau^{(1)}_{\epsilon \text{err}}}.
\]

Similarly, if \( \Lambda^{(2)}(\cdot) \) in (9) is used in the FSS test (10), it can be shown that both of the verification error probabilities are bounded from above by the quantity

\[
\left( \min_{\epsilon \in [0, 1]} \int_{-\infty}^{\infty} [\Lambda^{(2)}(y)]^{4} \left[ \phi(y - p) + \phi(y + p) \right] dy \right)^{\tau^{(2)}_{\epsilon \text{err}}}.
\]

for any fixed \( \epsilon \in [0, 1] \). Let \( \rho^{(\ell)} \), \( \ell = 1, 2 \) denote the minimum quantity in the large parentheses in (11) and (12), respectively. Then it can be shown that \( \rho^{(1)} < 1 \), so the Chernoff bounds (11), (12) on the error probabilities converge to zero exponentially in the number of observations used. Thus, for any specified error probability \( \text{Pe}_{\text{err}} \), choosing \( T^{(\ell)}_\text{err} \) such that

\[
T^{(\ell)}_\text{err} \geq \frac{\log_{10} \text{Pe}_{\text{err}}}{\log_{10} \rho^{(\ell)}}
\]

satisfies the given specification. The quantity \( \rho^{(\ell)} \) can be obtained numerically via the Newton-Raphson method.

Unfortunately, the verification stage discussed above can not be directly applied to an actual serial search scheme for the chip-asynchronous model. This is due to a slight problem under the out-of-phase hypothesis \( H_0^{(2)} \) in (4) when \( k = i - 1 \). In this situation, the observations take on only of two possible mean values \( p \) and \( -(1 - 2\epsilon)p \), rather than one of the four possible values \( \pm p \) and \( \pm (1 - 2\epsilon)p \) corresponding to \( H_0^{(2)} \) in (5). Indeed, note from (4) that if \( k = i - 1 \) and \( \epsilon \approx 1 \), the mean values are all very nearly

1177

36.3-3
p, and it appears that the in-phase hypothesis $H_2$ is true. Thus, due to this problem when $k = i - 1$, we cannot guarantee that the error probabilities incurred at the verification stage do not exceed the specification $P_{ver}$ (note that the specification is satisfied at all phase cells with $k \neq i - 1$). However, we design a modified verification procedure as follows such that the verification error probabilities do not exceed $2P_{ver}$, and this is the case for any $k$ and $i$.

It is convenient to modify the random sequence model in (5) in order to handle the case where $k = i - 1$ in (4). To this end, we define two new hypotheses $H_0^{(1)}$ and $H_1^{(1)}$, where $H_0^{(1)}$ is used to model $H_0$ when $k = i - 1$ in (4), and $H_1^{(1)}$ is used to model $H_0$ when $k \neq i - 1$ and $k \neq i$. Thus, we obtain the modified random sequence model for $\{Z(j): j \in S_i\}$ given by

$$Z(j) = \begin{cases} p + W(j) & \text{if } k = i, \text{ i.e., if } H_0^{(1)} = H_1 \\
p X(j) + W(j) & \text{if } k = i - 1, \text{ i.e., if } H_0^{(1)} = H_0 \\
p X(j) + W(j) & \text{otherwise, i.e., if } H_0^{(1)} = H_0^{(1)} \end{cases}$$

(14)

where $X(j)$ takes each of the two values $+1$ and $-(1 - 2e)$ with equal probability independently of $\{W\}$, and, as before, $X(j)$ takes each of the four values $\pm 1$ and $\pm (1 - 2e)$ with equal probability independently of $\{W\}$. Thus, the hypothesis $H_0$ in (4) is modeled as being either $H_0^{(1)}$ or $H_0^{(1)}$ depending on whether or not $k = i - 1$. Note that when $k \neq i - 1$, $H_0^{(1)}$ in (14) is the same as $H_0^{(1)}$ in (5).

We now obtain a modified verification stage for which the verification error probabilities do not exceed $2P_{ver}$ under any of the three possible hypotheses in (14). Suppose that the current local PN phase used at the testing stage is $i$, and that the testing stage has decided that the in-phase hypothesis $H_0^{(1)} = H_1$ is true, i.e., that $k = i$. In order to verify whether this decision is correct, the proposed verification stage employs two tests in parallel. One of these tests correlates with the local phase $i$ and uses the observations $\{Z(j): j \in S_i\}$ in a FSS test as described earlier. The other test correlates with the local phase $i - 1$ and uses the observations $\{Z(j): j \in S_{i-1}\}$ in a FSS test. Let $T_r$ and $T_{ver}$ denote these FSS tests. Then our verification procedure is described as follows:

- If $T_r$ rejects the phase $i$, then reject the hypothesis that $k = i$ and resume the serial search at the next phase cell $i + 1$.
- If $T_r$ accepts the phase $i$ and $T_{ver}$ rejects the phase $i - 1$, then accept the hypothesis that $k = i$ and terminate the serial search.
- If $T_r$ accepts the phase $i$ and $T_{ver}$ accepts the phase $i - 1$, then accept the hypothesis that $k = i - 1$ and terminate the serial search.

The error probabilities incurred by this verification procedure are assessed as follows under each of the three hypotheses in (14). Define the events $VE = \{\text{verification error}\}$, $V_i = \{T_r \text{ accepts the phase } i\}$, $V_{i-1} = \{T_{ver} \text{ accepts the phase } i - 1\}$, and write $V^c$ as the complement of $V$. Suppose that $H_0^{(1)} = H_2$ is true, that is, $k = i$. Then we have

$$P(VE|H_0^{(1)}) = P(V_i \cup V_{i-1})|H_0^{(1)})$$

$$= P(V_i|H_0^{(1)}) + P(V_{i-1}|H_0^{(1)})$$

$$\leq P_{ver} + P_{ver} = 2P_{ver},$$

(15)

where the last inequality follows since $k = i$ under $H_0^{(1)}$ and each verification test satisfies the specification $P_{ver}$ in this case. In a similar manner, it can be shown that the verification error probability does not exceed $2P_{ver}$ under $H_0^{(1)}$ and $H_0^{(1)}$. Thus, the error probabilities incurred by the proposed verification procedure do not exceed $2P_{ver}$, where $P_{ver}$ is the specification used to design the individual FSS tests described earlier. Moreover, this result is valid for any $e \in [0, 1]$. As an example of the verification stage design, consider the case where the overall verification error probability specification is $10^{-8}$. Thus, we design the FSS tests via (11)-(13) with the specification $P_{ver} = 10^{-8}/2$. Some numerical results for this case are shown in Table 1. Note that the test based on the zero sequence model requires more observations than does the test based on the random sequence model. These values will be used in Section 5 to compute the mean acquisition time of the schemes considered.

5 Comparison of Mean Acquisition Time

We consider the mean acquisition time $E[T_{acq}]$ of the serial search acquisition scheme under the chip-asynchronous model described above. The testing stage employs an SPRT as described in Section 3, and the verification stage uses a FSS test as described in Section 4. The state diagram for the serial search acquisition scheme under the chip-asynchronous model is shown in Figure 1, where $k$ is the phase of the incoming sequence and $L'$ is the number of phases in the uncertainty region. The observations available at the receiver are assumed to be distributed according to the modified random sequence model as in (14), i.e., the spreading sequences appearing under the out-of-phase hypothesis are modeled as random sequences. We assume that the error probability specification $P_{ver}$ in the verification stage is sufficiently small, so that the operation of the verification stage is virtually error free and that the acquisition stage $ACQ$ in Figure 1 is reached with (virtual) probability one. Then, the mean acquisition time $E[T_{acq}]$ is defined as the average time required to reach the acquisition stage $ACQ$, measured in units of the chip duration $T_c$. Since the observations are i.i.d. under each of the three hypotheses in (14) and the unknown phase $k$ is uniformly distributed over the uncertainty region, it can be shown [7] that

$$E[T_{acq}] = \frac{1}{L'} \left( \frac{1 + (L'-1)}{1 - \beta(1 - \hat{\alpha})} \right) [E_0[N] + \alpha(1 - \hat{\alpha})T_{ver}] + (1 - \hat{\alpha})L'(L'-2)E_0[N] + (1 - \hat{\alpha})E_1[N]$$

$$+ \frac{1}{L'} \left( \frac{(L'-1)(L'-2)}{2} \right) [E_0[N] + \alpha T_{ver}]$$

$$+ \left( L' - 1 \right) E_1[N] + T_{ver},$$

(16)

where $\alpha, \hat{\alpha}$ and $\beta$ are the probabilities of false alarm and missed detection at the testing stage, respectively, $E_0[N], E_1[N]$ and $E_1[N]$ are the ASNs, and $T_{ver}$ is the fixed number of observations processed at the verification stage. Note that $\hat{\alpha}$ and $E_0[N]$ are different from $\alpha$ and $E_0[N]$, and arise from the phase cell corresponding to $i = k + 1$, as can be seen from the state diagram in Figure 1. That is, $\hat{\alpha}$ and $E_0[N]$ denote the performance parameters under the hypothesis $H_0^{(1)}$ in (14), while $\alpha$ and $E_0[N]$ denote the performance parameters under $H_2^{(1)}$ in (14) (and also $H_0^{(1)}$ in (5)).

Now, we wish to compare $E[T_{acq}]$ for the two acquisition schemes considered, namely, the schemes whose testing and veri-
fication stages are based both on the random sequence and zero sequence models, when the observations are distributed according to (14) for some fixed values of $c$ and $p$. To do this, we evaluate (16) with $\alpha = \alpha(t)$, $\beta = \beta(t)$, $E_0[N] = E_0^1[N(t)]$, $E_0[N] = E_0^2[N(t)]$, $E_1[N] = E_1^1[N(t)]$, and $T_{ter} = T_{ter}^1$ for $t = 1, 2$, where the various parameters were defined in Sections 3 and 4. Note that the error probabilities and ASNs of the SPRTs depend on the thresholds $A(t)$ and $B(t)$, and these thresholds still need to be selected. Often it is the case that nominal error probabilities $a_0$ and $b_0$ are given, and one wishes to select the thresholds which approximately achieve this performance. The standard way of doing this is to use the thresholds

$$A(t) \cong \frac{b_0}{1 - a_0},$$

$$B(t) \cong \frac{1 - b_0}{a_0},$$

(17)

as described in [3, 5]. Once the thresholds are specified, the error probabilities and ASNs for the SPRTs are computed for different values of $p$ using the iterative numerical method described in [7]. Then, $E[T_{rea}]$ in (16) may be computed from these results and those in Table 1.

The cases we consider are for $L = 1023$ with $a_0 = b_0 = 0.01$, and we assume the thresholds are chosen as in (17). The results for $E[T_{rea}]$ are shown in Figures 2, 3, and 4 as a function of $p$ when $\epsilon = 0, 0.5$, and 0.9, respectively, where the chip SNR $p/2$ is in the range $-17$ dB to $-3$ dB. In general, the acquisition scheme based on the random sequence model has a smaller mean acquisition time than does the acquisition scheme based on the zero sequence model. As for the chip synchronous model studied in [4], the difference between the $E[T_{rea}]$ performance of the two schemes becomes more significant for larger values of $p$, due to the fact that the likelihood ratio for the zero sequence model test becomes severely mismatched from the true distribution under the out-of-phase hypothesis when $p$ is large. Also note from Figures 2-4 that the $E[T_{rea}]$ performance varies depending on the value of $\epsilon$, and that the scheme based on the zero sequence model performs best when $\epsilon = 0.5$. This is not surprising, since the likelihood ratio for the zero sequence model test is best matched to the true distribution of the observations when $\epsilon = 0.5$ [5, 7].

The results indicate that the performance of the scheme based on the random sequence model is relatively insensitive to the value of $\epsilon$. Hence, the scheme based on the random sequence model is robust in terms of mean acquisition time performance for any value of $\epsilon$. Moreover, for moderate to large value of chip SNR, the search scheme based on the random sequence model offers considerable savings in mean acquisition time over the search scheme based on the zero sequence model. These trends were also generally observed in [7] where other parameter choices were considered.

As a final remark, we point out that the actual mean acquisition time for the serial search scheme is twice the value in (16). The reason for this is that both the SPRT in the testing stage and the FSS in the verification stage use only the observations $\{Z(j) : j \in S_i\}$, and these are only half of all the available observations under the random sequence model. The benefit in using this partial observation strategy is that the in-phase hypothesis $H_1$ is reduced to a simple hypothesis, so that there is no performance degradation under $H_1$ due to unknown $\epsilon$ or the use of actual PN sequences. Schemes which use all of the observations in the testing stage were briefly considered in [7].

6 Conclusions

A novel serial search acquisition scheme was proposed for use in chip-asynchronous DS/SS systems. Only a subset of the available observations was utilized to test for the phase $k$ of the received sequence. The testing stage was briefly summarized, and an appropriate verification stage with FSS tests was designed to satisfy an arbitrary error probability specification for any realization of the unknown parameter $\epsilon$. The various tests were based on random sequence and zero sequence models for the sequences arising under the out-of-phase hypothesis. The mean acquisition time $E[T_{rea}]$ was derived for these schemes when the out-of-phase sequences are random sequences. Our results show that if the SNR is sufficiently small, a simple correlator statistic based on the zero sequence model yields $E[T_{rea}]$ performance which is very similar to that obtained by use of the statistic based on the random sequence model. On the other hand, for moderate to large values of SNR, the test statistic based on the random sequence model offers considerable savings in mean acquisition time.

ACKNOWLEDGEMENT

This research was supported in part by the Joint Services Electronics Program under Grant No. N00014-90-J-1270.

References