

Signal Processing Seminar

Title: A Communications-inspired Design Paradigm for Nanoscale Systems-on-a-chip

Speaker: Professor Naresh Shanbhag
University of Illinois

Date: Wednesday, September 9, 2009

Time: 4:00 - 5:00 pm

Where: 4269 Beckman Institute

Abstract: Moore's Law has been the driving force behind the exponential growth in the semiconductor industry for the past 4 decades. Today, power and reliability challenges threaten the continuation of Moore's Law. This talk will describe a communications-inspired design paradigm for nanoscale SOCs which has the potential to provide an elegant solution to the power-reliability problem. This design paradigm views nanometer SOCs as miniature communication networks, and exploits the principles of reliable information transfer developed by communication system designers and information theorists over the past six decades. Key elements of this paradigm are the use of statistical signal processing principles, equalization and error-control for designing error-resilient on-chip computation, communication, storage, and mixed-signal analog front-ends. The talk will provide a historical perspective, demonstrate examples of communications-inspired designs of on-chip sub-systems such as low-power filtering, video compression, PN-code acquisition, and on-chip and off-chip interconnect design, describe other on-going research at UI, and within the broader research community such as the MARCO Gigascale Systems Research Center (GSRC). The seminar will conclude with an invitation to signal processing researchers and system theorists to collaborate with circuit designers in order to address this important problem.

Speaker Bio: Naresh R. Shanbhag received his Ph.D. degree in EE from the University of Minnesota in 1993. From July 1993 to August 1995, he worked in AT&T Bell Laboratories at Murray Hill, New Jersey, where he was responsible for the development of VLSI algorithms, architectures and implementation of broadband data communications transceivers. In particular, he was the lead chip architect for AT&T's 51.84 Mb/s transceiver chips over twisted-pair wiring for Asynchronous Transfer Mode (ATM)-LAN and very high-speed digital subscriber line (VDSL) chip-sets. Since August 1995, he is with the Department of Electrical and Computer Engineering, and the Coordinated Science Laboratory where he is presently a Professor.

Dr. Shanbhag's research focuses on two major areas: the design of VLSI chips for broadband communications and the design of energy-efficient and reliable VLSI chips employing communication system design principles. He has published more than 90 journal articles/book chapters/conference publications in this area and holds three US patents. He is also a co-author of the research monograph *Pipelined Adaptive Digital Filters* published by Kluwer Academic Publishers in 1994.

Dr. Shanbhag is a co-founder (along with Dr. Singer) and Chief Technology Officer of Intersymbol Communications, Inc., a venture-funded fabless semiconductor start-up that provides mixed-signal ICs for electronic dispersion compensation for optical links. Intersymbol Communications, Inc., was acquired by [Finisar Corporation](#) in 2007, where Dr. Shanbhag also serves as a Sr. Scientist on a part-time basis.